line 1083 is fed from V_{PG} which is in turn supplied by the controller from a line 1901. Figure 27 shows V_{PG} to assume various voltages under different functions of the EEprom.

The variability of V_{CG} is particularly advantageous in program and erase margining schemes. In program margining, the read during program verify is done with V_{CG} at a slightly higher voltage than the standard V_{cc}. This helps to place the programmed threshold well into the state by programming past the breakpoint threshold level with a slight margin. In erase verify, the cell is verified with a somewhat reduced V_{CG} to put the cell well into the "erased" state. Furthermore, margining can be used to offset the charge retention problem described earlier (Figure 16B).

As mentioned before, prior art EEproms typically employ V_{cc} to feed V_{CG} during program or erase verify. In order to do margining, V_{cc} itself needs to be ramped up or reduced. This practice produces inaccurate results in the reading circuits since they are also driven by V_{cc}.

In the present invention, the variability of V_{CG} independent of voltages supplied to the reading circuit produce more accurate and reliable results.

Furthermore, the wide range of V_{CG} is useful during testing and diagnostic of the EEprom. It allows the full range of the programmed cell's threshold to be measured easily by continuing to increase V_{CG} (up to the maximum limited by the device's junction breakdown).--

IN THE DRAWINGS:

Add the accompanying sheets 6-22 of drawings, in informal form, which contain additional Figures 9-27.

IN THE CLAIMS:

Please cancel the original parent application claims 1-62, without prejudice, and substitute the following new claims therefore:

--63. A method of operating an EEprom system having memory cells that individually include an electrically floating gate carrying a charge level that is alterable in response to appropriate voltages applied to the cell, thereby to establish a

variable threshold level that is detectable upon reading the cell, said method comprising:

applying said appropriate voltages to a plurality of said memory cells in parallel, thereby to alter the charge levels on the floating gates of said plurality of memory cells,

individually detecting the threshold levels of said plurality of memory cells, and

terminating said application of appropriate voltages to individual ones of said plurality of memory cells as soon as they are detected to have reached desired threshold levels while continuing to apply said appropriate voltages to others of said plurality of cells until all of the plurality of cells are detected to have reached desired threshold levels.

64. The method of claim 63, wherein there are exactly two of said desired threshold levels.

65. The method of claim 63, wherein there are more than two of said desired threshold levels.

66. The method of claim 63, wherein said desired threshold levels of the plurality of memory cells include exactly two non-overlapping programmed ranges of threshold levels.

67. The method of claim 63, wherein said desired threshold levels of the plurality of memory cells include more than two non-overlapping programmed ranges of threshold levels.

68. The method of claim 63, wherein said desired threshold levels include an erased threshold level.

69. The method of claim 63, wherein the array of memory cells are grouped into blocks of cells whose threshold levels are changed together to a single given level prior to applying the appropriate voltages.

70. The method of claim 69, wherein said plurality of memory cells to which said appropriate voltages are applied in parallel are less than a number of memory cells within individual ones of said blocks, and additionally comprising repeating for another plurality of cells within one of said blocks said applying, detecting and terminating operations.

71. The method of claim 69, wherein ~~individual~~ ones of the blocks of cells ~~contain~~ a number of spare cells to which the